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EXAMINER	
HILTUNEN, THOMAS J	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 11/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/776,354	ARMSTRONG ET AL.	
	Examiner	Art Unit	
	Thomas J. Hiltunen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-17 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-17 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112, second paragraph

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 16 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is unclear what the recitation of "its" refers to on lines 6 and 10.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3, 5, 11-12, 15 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Mizuno et al. (USPN 6,166,577).

With respect to claim 1, Mizuno et al. discloses in Fig. 4, "a method for actively adjusting the back bias voltage of one or more CMOS transistors comprising the steps:

fabricating a reference transistor on a chip (the transistors of OSC1 are fabricated to output a reference signal S1 to substrate bias control circuit CNT1),

monitoring the leakage current of the reference transistor with an active dc output control circuit (CNT 1 monitors the difference between the leakage current of OSC1, by having output line S1 of OSC1 connected to phase/frequency detector PFD1, which compares the difference between S1 and CLK1), and

adjusting the back bias voltage of the well containing the reference transistor until the leakage current is below a preset value (CNT1 detects when S1 is lower than CLK1, and then outputs BP1 and BN1 to adjust the back bias voltages of the transistors OSC1, and Log1 (See Col. 8 lines 44-55), by having BP1 and BN1 connected to the back gate of the transistors of OSC1 and LOG1. This is done to "minimize the power consumption caused by the subthreshold leakage current" (Col. 3 lines 60-66 disclose that it is possible to use the circuit for the minimization of leakage current)."

With respect to claim 3, Mizuno et al. discloses in Fig. 4, "the method of claim 1 wherein said monitoring and said adjusting are performed by an active dc output control circuit not on the same chip as the reference transistor (It can be seen that OSC1 and CNT1 are on different chips.)."

With respect to claim 5, Mizuno et al. discloses in Fig. 12, "the method of claim 1 wherein there is one or more active dc output control circuits on the same chip with one or more reference transistors (it can be seen that there are multiple control circuits CNT10-30, and multiple reference transistor circuits OSC10-30, in which the whole circuit of Fig. 12 can be integrated on a chip. Additionally, Col. 15 lines 9-17 disclose how to integrate circuit 12 on a "semiconductor chip".)."

With respect to claim 11, Mizuno et al. discloses in Fig. 4, "an integrated circuit for actively adjusting the back bias voltage of one or more CMOS transistors comprising:

a means for monitoring the leakage current of a reference transistor (transistors of OSC1) on a chip (it can be seen that CNT1 monitors the leakage current with PFD1, by comparing the output of OSC1 (S1) with CLK1),

a means for adjusting the back bias voltage of the well containing the reference transistor (BGEN1 adjusts the back bias voltage of the transistors of OSC1),

a means for determining when the leakage current is below a preset value (PFD1 determines when S1 is below CLK1), and

a means for maintaining the back bias voltage and the leakage current in a narrow range (BGEN1 maintains back bias voltage of OSC1 and LOG1 in order to keep the subthreshold leakage current minimized)."

With respect to claim 12, Mizuno discloses in Fig. 4, "the integrated circuit of claim 1, wherein said integrated circuit is not on the same chip as the reference transistor (it can seen that OSC1 are the control circuit are separate from each other)."

With respect to claim 15, it can be seen in Fig. 4 Mizuno et al. discloses adjusting the back bias of both the OSC1 transistors and the LOG1 transistors. The LOG1 and OSC1 transistors don't share the same well. Thus BGEN1 adjusts "the back bias of a well (connected to the backgate of the transistors of the LOG1 circuit) not containing the reference transistor."

With respect to claim 17, Mizuno et al. discloses in Fig. 4, "an integrated circuit for actively adjusting the threshold voltage of one or more CMOS transistors comprising:

a means for monitoring the leakage current of a reference transistor on a chip (PFD1);

a means for adjusting the back bias voltage of the well containing the reference transistor (BGEN1);

a means for determining when the leakage current is about a preset value (PFD1 monitors when S1 is below CLK1);

a means for maintaining the back bias voltage and the leakage current in a narrow range (BGEN1 maintains the back bias voltage of OSC1 and LOG1 to maintain a minimized leakage current);

and a means for correlating said leakage current with the threshold voltage (threshold voltage and leakage current are correlated, "when the threshold voltage is set too low, the MOS transistor cannot turn off completely due to subthreshold characteristics, causing a subthreshold leakage current to flow (Col.1 lines 16-20). Thus Mizuno et al. discloses a negative correlation between threshold voltage and leakage current (i.e. when threshold voltage decreases, leakage current increases). Therefore when the threshold voltage of the transistors of OSC1 or LOG1 decreases the leakage current will increase)."

Claims 1, 7-10, 11, 14 and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Miyazaki et al. (USPN 6,489,833).

With respect to claim 1, Miyazaki et al. discloses in Fig. 2, "a method for actively adjusting the back bias voltage of one or more CMOS transistors comprising the steps:

fabricating a reference transistor on a chip (the transistors of DMON01(see fig. 5 DMON11 is composed of PMOS and NMOS transistors) are fabricated to output a reference signal inv01 to substrate bias control circuit CMP01),

monitoring the leakage current of the reference transistor with an active dc output control circuit (CMP01 monitors the difference between the leakage current of DMON01, by receiving inputs of inv01 and CLK02 which allows CMP01 to compare the difference between inv01 with respect to clk02), and

adjusting the back bias voltage of the well containing the reference transistor until the leakage current is below a preset value (SBG01 detects when up01 is lower than dw01, and then outputs vbp01 and bbn1 to adjust the back bias voltages of the transistors DMON01, and LOG01. The back bias voltages of DMON01 and LOG01 are adjusted to limit the leakage current to a minimum value, and to maintain constant operating speeds, see Col. 7 lines 57-67 and Col. 8 lines 1-5)."

With respect to claim 7, Miyazaki et al. discloses, "the method of claim 1 wherein, said preset leakage value is stored in programmable circuit elements of said active dc output control circuit after fabrication (In Fig. 6 it can be seen that the COMP01 is composed of flip-flops, which are programmed to maintain the level present at D until inva and invb change states with respect to clkb.)."

With respect to claim 8, Miyazaki et al., discloses, "the method of claim 7 wherein said preset leakage value is stored in re-programmable circuit elements of said active

dc output control circuit after fabrication (The latches are reprogrammable when reset signal clka, or when the output of and11 or and12 are a "high" value.)."

With respect to claim 9, Miyazaki et al., discloses,."the method of claim 8 wherein said active dc output control circuit processes a signal to set said preset leakage value in said reprogrammable circuit elements of said active dc output control circuit (it can be seen that COMP01 receives inv01 and clk02. Clk02 is sets the level of the preset leakage value. Thus the flip-flops of COMP11 of Fig. 6 process the signal that sets the preset leakage value.)."

With respect to claim 10, Miyazaki et al., discloses, "the method of claim 9 wherein said active dc output control circuit contains re-programmable circuit elements and addressing means for one or more preset leakage values (The lines that connect clk(a-c) to the flip-flops of Fig. 6 are the means for addressing the flip-flop (memory devices))."

With respect to claim 11, Miyazaki et al. discloses in Fig. 2, "an integrated circuit for actively adjusting the back bias voltage of one or more CMOS transistors comprising:

a means for monitoring the leakage current of a reference transistor (transistors of DMON01) on a chip (it can be seen that CMP01 monitors the leakage current with, by comparing the output of DMON01 (inv02) with CLK02),

a means for adjusting the back bias voltage of the well containing the reference transistor (SBG01 adjusts the back bias voltage of the transistors of DMON01),

a means for determining when the leakage current is below a preset value (CMP01 determines when inv01 is below CLK02), and

a means for maintaining the back bias voltage and the leakage current in a narrow range (SBG01 maintains back bias voltage of DMON01 and LOG1 in order to minimize the subthreshold leakage current and maintain constant operating speeds (See Col. 7 lines 62-67 and Col. 8 lines 1-5)."

With respect to claim 14, Miyazaki et al. discloses, the leakage current of circuit DMON01 being input to storage device CMP01 containing flip-flop devices (see Fig. 6), which hold a value until the clock signal becomes high.

With respect to claim 16, Miyazaki discloses in Fig. 6, "an integrated circuit for actively adjusting one or more of its output voltages based on monitoring the current of one or more CMOS transistors comprising;

a means for monitoring the current of one or more CMOS transistors (transistors of DMON01),

a means for adjusting one or more of its output voltages (SBG01),

a means for determining when the monitored one or more currents is below a preset value (CMP01),

a means for maintaining its one or more output voltages in a narrow range (SBG01 maintains voltages vbp01 and vbn01 in a narrow range to reduce leakage current, and keep operating speeds constant. See Coll. 7 lines 57-63),

a means for storing the preset values in programmable memory (the flip-flops of CMP11 in Fig.6)."

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 7-10,11,14, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsunoda et al. (6,654,305) in view of Mizuno et al. (6,166,577). Tsunoda et al. teaches a substrate-bias generation circuit with a control value storage unit. Tsunoda et al. does not teach the specifics of the substrate-bias generation circuit. Mizuno et al. teaches the specifics of the substrate-bias generation circuit (see rejections of claims 1,3,5,11-12, and 17 above).

It would have been *prima facie* obvious to one of ordinary skill in the art at the time the invention was made to replace the generic substrate-bias generation and circuits of Tsunoda et al. with the specific substrate-bias generation circuit of Mizuno et al. (i.e. replacing com control 420 of Tsunoda et al. with MCU1 of Mizuno et al., Control circuit 460 of Tsunoda et al. with PILL1, PFD1 and LPF1 of Mizuno et al., substrate-bias generation circuit 300 of Tsunoda et al., with BGEN1 of Mizuno et al., and 200 of Tsunoda et al. with OSC1 and LOG1 of Mizuno et al.) for the purpose of having a simply constructed substrate-bias generation circuit. One skilled in the art would have been motivated to combine the circuits of Tsunoda et al. and Mizuno et al. with a reasonable expectation of success.

With respect to claim 1, see the rejection of claim 1 with respect to Fig. 4 of Mizuno et al. above.

With respect to claim 7, the above combination of Tsunoda et al. and Mizuno et al., discloses, "the method of claim 1 wherein, said preset leakage value is stored in programmable circuit elements of said active dc output control circuit after fabrication (the output of 200 is input into storage unit 430 of the control circuit 400. The memory would not store values until the circuit is fabricated and operated for the first time.)"

With respect to claim 8, the above combination of Tsunoda et al. and Mizuno et al., discloses, "the method of claim 7 wherein said preset leakage value is stored in re-programmable circuit elements of said active dc output control circuit after fabrication (450 is reprogrammable memory The memory would not store values until the circuit is fabricated and operated for the first time.)."

With respect to claim 9, the above combination of Tsunoda et al. and Mizuno et al., discloses, "the method of claim 8 wherein said active dc output control circuit processes a signal to set said preset leakage value in said reprogrammable circuit elements of said active dc output control circuit (the control circuit 460 processes the values stored in memory circuit 430)."

With respect to claim 10, the above combination of Tsunoda et al. and Mizuno et al., discloses, "the method of claim 9 wherein said active dc output control circuit contains re-programmable circuit elements and addressing means for one or more preset leakage values (the registers 440 are used to address one or more of the preset values in the memory 450 of storage device 430)."

With respect to claim 11, see the rejection of claim 11 with respect to Fig. 4 of Mizuno et al. above.

With respect to claim 14, the combination of Tsunoda et al. and Mizuno et al. discloses, the leakage current of circuit 200 (of Tsunoda et al.) being input to storage device 430 containing memory 450.

With respect to claim 16, the combination of Tsunoda et al. and Mizuno et al. discloses, "an integrated circuit for actively adjusting one or more of its output voltages based on monitoring the current of one or more CMOS transistors comprising;

a means for monitoring the current of one or more CMOS transistors (460 monitors the CMOS transistors of OSC1 of Mizuno et al. now in place of 200 of Tsunoda et al. (PFD1 which is in place of 460 would receive S1 from 200 output on line 230),

a means for adjusting one or more of its output voltages (300 adjusts 310n and 310p),

a means for determining when the monitored one or more currents is below a preset value (460 detects when the output of 200 is below CLK1 of Mizuno et al.),

a means for maintaining its one or more output voltages in a narrow range (300 is replaced by BGEN1 of Mizuno et al., BGEN1 maintains the back bias voltage of OSC1 and LOG1 (circuit 200 of Tsunoda et al.) to maintain a minimized leakage current),

a means for storing the preset values in programmable memory (storage device 430 contains programmable memory 450)."

Claims 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over in view of Mizuno et al. (6,166,577). Mizuno et al. discloses the circuit of claim 1. Mizuno et al. does not disclose the fabrication of the mask of the DC control circuit. However, Mizuno et al discloses in Col. 1 lines 24-33 that it is notoriously well known in the art that there is a correlation between "MOS transistor pattern design" (i.e. mask), and threshold voltage. Additionally, in Col. 1 lines 16-20 Mizuno et al. discloses the correlation between threshold voltage and leakage current (i.e. too low threshold voltage causes an increase in leakage current). Since it is well-known that mask design has an affect on threshold voltage it would be obvious to one of ordinary skill in the art that the mask design of the control voltage has an affect on the preset leakage value. Thus one would design the mask of the control circuit to be optimized, which would keep the preset leakage value from fluctuating form the desired CLK1 signal.

With respect to claim 6, Mizuno et al. discloses, "the method of claim I wherein said preset leakage value is determined by the mask design of said active dc output control circuit (the optimized mask design helps determine a more accurate comparison between CLK1 and S1)."

Claims 2, 4 and 13, are rejected under 35 U.S.C. 103(a) as being unpatentable over Mizuno et al. (6,166,577) in view of Dozza et al.
(USPN 6,292,400).

Mizuno et al. teaches the circuits of claim 1 in Fig. 4. Mizuno et al. does not

teach in Fig. 4 how the transistors of the circuit are fabricated. However, Dozza et al. discloses in Fig. 4, a NMOS transistor in a N-well. It would be obvious to one of ordinary skill in the art to fabricate a PMOS transistor the same way except reversing the type (N to P and P to N) of the wells and substrates of Fig. 4, because of the complementary nature of CMOS technology.

With respect to claim 2, the combination of Mizuno et al. and Dozza et al. discloses, "the method of claim 1 wherein said reference transistor (NMOS and PMOS transistors of OSC1 of Mizuno et al.) comprises a P-MOS transistor in a P-MOS well (due to CMOS technology the PMOS transistors of OSC1 would be like Fig. 4 of Dozza et al., except have PMOS transistor in a PMOS well) the or a N-MOS transistor in a N-MOS well (Dozza et al. shows a NMOS transistor in a NMOS well)".

With respect to claim 4, the combination of Mizuno et al. and Dozza et al. discloses, the method of claim 1 wherein said active dc output control circuit monitors and adjusts at least one P-MOS well and at least one N-MOS well (It can be seen that S1 is connected to the drains of the PMOS and NMOS transistors, thus CNT1 monitors a NMOS well and a PMOS well, and controls the well connected to the backgate of the NMOS and PMOS transistor of OSC1.)."

With respect to claim 13, the combination of Mizuno et al. and Dozza et al. discloses, "the integrated circuit of claim 1 wherein said reference transistor (NMOS and PMOS transistors of OSC1 of Mizuno et al.) comprises a P-MOS transistor in a P-MOS well (due to CMOS technology the PMOS transistors of OSC1 would be like Fig. 4 of Dozza et al., except have PMOS transistor in a PMOS well) the or a N-MOS transistor

in a N-MOS well (Dozza et al. shows a NMOS transistor in a NMOS well)".

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kojima (USPN 6,670,678) discloses in Fig. 7 and Fig. 8 a PMOS transistor in a substrate and a NMOS transistor in a NMOS well.

Bertin et al. (USPN 6,433,618) discloses in Fig. 1 multiple reference transistors and a back bias control circuit.

Tsay et al. (USPN 6,239,650) discloses a detection leakage current detection circuit and a back bias control circuit.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Hiltunen whose telephone number is (571) 272-5525. The examiner can normally be reached on Mondays - Fridays from 8:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan, can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TH
November 14, 2005

Terry D. Cunningham
Primary Examiner
Art Unit 2816